REMARKS

The Office Action dated October 25, 2006 has been received and carefully considered. In this response, claims 15-19 have been withdrawn from prosecution. Entry of the withdrawal of claims 15-19 is respectfully requested. Reconsideration of the outstanding rejections in the present application is also respectfully requested based on the following remarks.

I. THE DOUBLE-PATENTING REJECTION OF CLAIMS 1-14

On page 2 of the Office Action, claims 1-14 were rejected under the judicially created doctrine of obviousness-type double-patenting as being unpatentable over claims in U.S. Patent Nos. 6,388,890 and 6,545,876 (hereinafter "the '890 patent" and "the '876 patent" respectively). This rejection is hereby respectfully traversed.

Since the Examiner did not identify the specific claims on which this double-patenting rejection is based, Applicants assume that the Examiner refers to method claims 1-14 in the '890 patent and method claims 2 and 19-34 in the '876 patent.

The above-identified method claims in the '890 patent and the '876 patent are directed to channel routing techniques, wherein vias in a first layer of a "multilayer signal routing device" may be arranged to create "channels" in a second layer.

Since the "channels" created based on the channel routing techniques are typically wider than a regular pitch between adjacent vias, signal runs (or conductive traces) may be more easily routed within these channels.

The currently pending claims 1-14 are related to the '890 patent and the '876 patent only to the extent that those earlier disclosed channel routing techniques may be employed here to form the (inter-component) channels by arranging vias in the multilayer signal routing device, as recited in claims 1 and 10. However, the currently pending claims recite more than the use of basic channel routing techniques, but also address signal routing among "a plurality of electronic components" based on inter-component channels that are arranged in different orientations. Therefore, the presently claimed invention is patentably distinct from the '890 patent and the '876 patent.

In view of the foregoing, it is respectfully requested that the aforementioned double-patenting rejection of claims 1-14 be withdrawn.

II. THE ANTICIPATION REJECTION OF CLAIMS 1-14

On page 3 of the Office Action, claims 1-14 were rejected under 35 U.S.C. § 102(b) as being anticipated by Carey et al.

(U.S. Patent No. 5,438,166, hereinafter "Carey"). This rejection is hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). Such possession is effected only if one of ordinary skill in the art could have combined the disclosure in the prior art reference with his/her own knowledge to make the claimed invention. Id.

Without individually addressing the pending claims, the Examiner makes the following assertions:

1) Carey discloses a plurality of channels (64);

2) col. 11, lines 45-46 discloses different orientations;

3) 44 and 46 are different components;

4) it is inherent that 50 are formed by forming vias through insulating layers and filling the vias with conductors;

5) col. 12, lines 61-63 discloses forming channels at different layers;

6) a blind via is formed between from conductors 50 to 51;

7) it is inherent that conductors are formed at different layers to different electronic components.

Office Action, page 3, paragraph 5. It is respectively submitted that the Examiner's citations to Carey have failed to show that Carey teaches or suggests all the elements presently claimed.

First, it is worth noting that Carey is directed to a completely different type of electronic product as compared to the "multilayer signal routing device" recited in the pending claims. Carey discloses a customizable circuitry having mass-produced wire segments forming programmable junctions. In other words, Carey's interconnect board have a fixed arrangement in terms of wire segments which typically constitute the majority of conductive traces in an interconnect board. The only things that ever change after the mass production of the interconnect board are the programmable links (e.g., 72) and vias (e.g., pillar 70). Once produced, no additional wiring (other than the inter-layer vias or links) can be added to or removed from

Carey's interconnect board. Accordingly, it is neither possible nor necessary to implement any channel routing technique in the customizable circuitry disclosed in Carey.

Second, the Examiner's understanding of Carey, as reflected in the above-listed citations, is either inaccurate or incorrect.

For example, the Examiner asserts that "Carey discloses a plurality of channels (64)." Yet, the channels (64) as shown in Figures 2-5 of Carey are different in many aspects from the "inter-component channel" presently claimed. The "inter-component channels" as recited in claims 1 and 10 refers to extra spacing created "for accommodating a plurality of conductive traces by arranging vias ... in the multilayer signal routing device."

On the other hand, the "channels (64)" in Carey are "programming tracks" "formed through and across the customization plane 48" such that "the underlying diagonally-extending programmable junctions 66 are accessible therethrough" (col. 11, lines 10-15). In other words, the so-called "channels (64)" are essentially cut-out portions of the customization plane that expose underlying programmable junctions for vertical access from the customization plane. The channels (64) are not formed by arranging or re-arranging vias, are not located in any

signal layer, and do not accommodate the routing of conductive traces. As such, the "inter-component channels" in the present invention are completely different from Carey's programming tracks in formation, location and function.

In addition, the Examiner's interpretation of the "programming tracks" as equivalent of the presently claimed "channels" is inconsistent with the Examiner's subsequent assertion that "col. 12, lines 61-63 discloses forming channels at different layers" (emphasis added). Col. 12, lines 61-63 in Carey reads:

> "In FIG. 8, solid lines indicate conductors in the upper conductor layer while dashed lines indicate conductors in the lower conductor layer."

Now, the Examiner appears to treat the X- and Y-conductor segments as "channels." In the same drawing, the programming tracks 64 are also shown.

Applicants respectfully submit that the conductor segments in Carey clearly cannot anticipate the "inter-component channels" as presently claimed. If the programming tracks in Carey were treated as "inter-component channels," they could not be formed at different layers, but are located in the same customization layer as illustrated in Figures 2-5.

The Examiner further points to Carey at col. 11, lines 45-46 ("... the tracks can assume any angle depending solely on

user needs.") as disclosing different orientations of "channels." Applicants respectfully disagree.

All the programming tracks shown in the Carey drawings are in parallel with one another. See, e.g., Figures 2-5, 8, 23 and 34. Carey never shows or describes any programming tracks (on a same interconnect board) that have different orientations or cross one another. Therefore, Carey meant to have parallel programming tracks that extend diagonally across the interconnect at the same angle. As confirmation, in the same paragraph cited by the Examiner, Carey describes a "pitch (P), as a measure of the distance between successive programming tracks" (col. 11, lines 49-51). It is well known that a "pitch" is meaningless unless the successive lines (or tracks) are evenly spaced. That is, the successive lines (or tracks) must be in parallel with each other, i.e., having the same orientation. Therefore, contrary to the Examiner's understanding, Carey does not contemplate programming tracks (let alone "channels") having different orientations.

The Examiner further states that "44 and 46 are different components." This statement may be true in the sense that wires 44 and 46 in Carey are two separate sets of wires. However, if the Examiner meant to read these "different components" onto the "plurality of electronic components" as recited in claims 1 and

10, the Examiner would be mistaken. The "electronic components" as presently claimed typically refers to integrated circuit (IC) chips that are mounted on a multilayer signal routing device, rather than the interconnecting wires themselves.

The Examiner's other assertions regarding the formation of vias do not appear to be particularly relevant to the anticipation rejection. While claims 1 and 10 recite "forming" "inter-component channels" by "arranging vias ... in the multilayer signal routing device," the Examiner's citations to Carey merely show that inter-layer vias are formed. Furthermore, the programming tracks, which the Examiner treats as the equivalent of "channels," are formed by cutting out portions of the customization plane, not by arranging or forming vias at all.

Third, in rejecting Applicants' method claims, it is improper for the Examiner to rely on structural features shown in Carey and supplement the deficiencies with "inherency" statements.

Claims 1 and 10 recite specific method steps for "routing one or more conductive traces between a plurality of electronic components of a multilayer signal routing device." In order for Carey to anticipate the present invention, Carey must teach or suggest the same or sufficiently similar method steps as

presently claimed. Such same or similar method steps would naturally tend to produce a same or similar end product. So far, however, the Examiner has not even shown that Carey creates a same or even similar multilayer signal routing device, let alone that Carey contemplates a same or similar method as presently claimed.

Accordingly, it is respectfully submitted that claims 1 and 10 are allowable over Carey.

Regarding claims 2-9 and 11-14, these claims are dependent upon independent claims 1 and 10 respectively. Thus, since independent claims 1 and 10 should be allowable as discussed above, claims 2-9 and 11-14 should also be allowable at least by virtue of their respective dependency on independent claims 1 and 10. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-14 be withdrawn.

III. CLAIM CHART

On page 4 of the Office Action, the Examiner requested references numerals to all the claimed limitations as well as

support in the disclosure for better clarity. In an attempt to fulfill this requirement, Applicants have provided reference numerals in claim 1 below. It is believed that independent claim 1 is representative of the present invention and reference numerals provided for claim 1 will assist the Examiner to better understand the claimed invention.

> 1 (Previously Presented). A method for routing one or more conductive traces between a plurality of electronic components of a multilayer signal routing device, the method comprising:
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> forming a first inter-component channel (**FIG. 1A-1B: 122A-C, 124A-C, 126A-C**) for accommodating a plurality of conductive traces (**FIG. 1B: 190, 192, 194**) at a first routing layer (**FIG. 2A: 124A-C; FIG. 2B: 122A-C, 124A-C, 126A-C**) of the multilayer signal routing device (**FIG. 1-2: 102A, 102B**), the first inter-component channel extending between a first set of two or more electronic components (**FIG. 1A: 104, 110 and 116 as one set**) of the plurality of electronic components (**FIG. 1-5: 104-120**) and having a first orientation (**FIG. 1A: vertical orientation of 122A-C, 124A-C, 126A-C**), the first inter-component channel formed by arranging vias (**FIG. 3: 306, 308, 316-320, 344**) for at least the first set of two or more electronic components in the multilayer signal routing device; and
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> forming a second inter-component channel (**FIG. 1A-1B: 128A-C, 130A-C and 132A-C**) for accommodating a

plurality of conductive traces (**FIG. 1B: 170-186**) by arranging vias at a second routing layer (**FIG. 2A: 128A-C, 130A-C and 132A-C; FIG. 2B: 130A-C**) of the multilayer signal routing device, the second inter-component channel extending between a second set of two or more electronic components (**FIG. 1A: 104, 106 and 108 as one set**) of the plurality of electronic components and having a second orientation different (**FIG. 1A: horizontal orientation of 128A-C, 130A-C and 132A-C**) from the first orientation, the second inter-component channel formed by arranging vias (**FIG. 3: 324**) for at least the second set of two or more electronic components in the multilayer signal routing device.

It should be noted that the reference numerals provided above are exemplary and do not constitute an exhaustive list of claimed features illustrated in the drawings.

IV. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the

present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

Hunton & Williams LLP

By: _____
Thomas E. Anderson
Registration No. 37,063

TEA/ccl

Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201

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